The Solido PVT+ package is a complete design debug and verification solution for corner-driven custom IC design. The package of applications provides everything designers need to quickly and comprehensively examine the whole PVT space, to extract the design-specific worst-case PVT corners, to identify PVT variation problems in the design, and to fix PVT variation problems effectively. PVT+ includes Fast PVT technology to minimize the number of simulations while accurately and comprehensively covering the full PVT space.

Each package offered by Solido offers the ability to analyze a circuit’s capabilities against the specification, to identify the electrical hotspots that have the greatest impact on performance, and to recommend design adjustments to meet the specification. With Solido PVT+, users quickly identify the worst-case PVT corners for use during design debug and then run Fast PVT for design sign-off. All this is done with capabilities to maximize simulator efficiency and minimize design verification time.

Benefits

**Fast**
- Extracts worst-case PVT corners 5-50x faster than running all combinations
- Predicts output values for the whole PVT space
- Parallelizes simulations across the compute cluster
- Dynamically stops when worst cases are found within accuracy tolerances

**Accurate**
- SPICE accurate results for worst cases
- Adaptively maximizes accuracy in worst-case regions
- Automatically self-verifies results
- Predicted values are accuracy-aware and include a confidence interval

**Scalable**
- Works for large PVT spaces with up to thousands of PVT corner combinations
- Produces even larger speed benefits with larger numbers of corners, while maintaining accuracy

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Featured Applications

Run PVT+
Run PVT+ quickly identifies the worst-case corners specific to the design being developed. Failures are automatically highlighted and the designer can easily see the PVT factors that create the biggest impact. The worst-case corners are easily extracted for use in Run DesignSense, which can then be used to identify the design changes that best meet all specifications across all PVT corners. By using design-specific worst-case PVT corners early in the design flow, the risk of failure in the final signoff is reduced. Run PVT+ provides additional benefit during final verification by analyzing the full set of PVT corner combinations, but only running a subset of simulations. Comprehensive PVT design verification can be completed with only a fraction of the simulations.

Run DesignSense
Identify the design hotspots with analysis of select devices against all design goals. DesignSense provides a clear indication of where design adjustments can be made to improve parametric performance, minimize sensitivity, reduce power, and minimize area.

DesignSense can be run at nominal or across the design-specific PVT corners extracted in Run PVT+. Users can quickly understand options to improve the design and the tradeoffs across all design goals.

Run Extracted Corners
Explore the effects of design changes on the performance of a design across selected standard or statistical corners. Track the design change history and the impact on the target specification.

Fast PVT vs Full-Factorial
Number of simulations for PVT validation

Specifications

Simulation management
• Support for LSF and SGE
• Simulation status monitor

Integration support
• ADE in IC 5.1.41
• ADE L in IC 6.1
• HSPICE compatible netlist

Simulation support
• Cadence - Spectre, APS
• Synopsys - HSPICE, HSIM
• Mentor - Eldo
• Berkeley DA - AFS
• Magma - FineSim

OS support
• RHEL 4, 5 - 32/64 bit
• SUSE 9, 10
• SPARC Solaris 10

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