Abstract
This report covers the results of an independent worldwide custom IC design survey. The survey was executed in late 2010, with 486 IC design professionals participating.

The Variation-Aware Custom Design report takes a closer look at trends associated with design variation, defined as the variation in parametric results caused by process and environmental (PVT), random variation, and layout dependent effects (parasitics, proximity). Its scope includes: general variation technology trends and factors in custom IC design; the impact of variation on project deadlines and financials; and adoption of commercial variation design systems.

The comprehensive feedback from custom IC designers and engineering management can be used to understand how variation is impacting semiconductor company management’s ability to meet design specifications and deadlines. This becomes especially critical with the increasing impact of variation with shrinking process geometries.

The topics covered in this report are:
1. Survey methodology and demographics
2. Custom IC areas where most advancement sought
3. Driving reasons for variation-aware design
4. Variation impact on project deadlines and tapeouts
5. Designer time spent managing variation
6. Plans to implement variation-aware design tools in 2011
7. Process nodes where variation-aware design becomes important
8. Ranking of custom IC design tools to be made “variation-aware”
9. Summary and financial Impact

1. Survey Methodology and Demographics
A blind, anonymous survey was emailed to several thousand participants worldwide by an independent consultancy over the time period from Sept 22, 2010 to November 7, 2010. 486 IC design professionals completed the survey online. Survey respondents were comprised of a broad spectrum of designers and engineering management, with a majority (53%) in an engineering management role.
2. Custom IC Areas where Most Advancement Sought

When asked to specify the segments of custom IC design where most technology advancement is needed within the next 2 years, the number one area identified was Variation-Aware Design (66%). The second tier of technologies specified were Parasitic Extraction (48%), Simulation (44%) and Physical Verification (40%). The third tier technology areas cited were Layout (26%) and Routing (24%). Schematic Capture showed only 7%.
3. Driving Reasons for Variation-Aware Custom Design
The top two reasons respondents gave for deploying variation-aware design systems were to improve parametric yield - performance, power and area (74%), and to avoid respins (64%). The secondary reasons noted were to avoid project delays (25%) and to save designer time (20%).

4. Variation Impact on Project Deadlines and Tapeouts
Variation issues are significantly affecting design delivery, with 53% of engineers and managers citing their organizations had missed a project deadline, delayed a tapeout, or required a respin due to variation problems.

For those who experienced project or tapeout delays due to design variation, the average length of delay cited was 2 work-months. The responses were normalized to find the average.
5. Designer Time Spent Managing Variation

Minimizing variation impact on parametric yield creates substantial additional overhead on design teams - designers spend an average of 22 percent of their time managing design variation.
6. Plans to Implement Variation-Aware Design Tools in 2011
Variation design is a rapidly growing factor in custom IC design. A total of 23 percent of design organizations indicate they already have variation-aware design tools deployed, and another 24 percent intend to implement this year. This result points to a 100 percent growth in organizational adoption of such tools in 2011.

7. Process Nodes where Variation-Aware Design Becomes Important
37 percent of designers and managers identified variation-aware design as becoming important when designing at a 90 nanometer process node. 60 percent saw 65 nanometers as necessary for design variation, and 85 percent saw it by 45 nanometers.
8. Ranking of Custom IC Design tools to be made “Variation-Aware”

Designers named the top existing custom IC design tools they wanted to be made “variation-aware” to be layout editors (66%), followed by true SPICE simulators (55%), fast SPICE simulators (52%), and then schematic capture (46%).

![Ranking of Tools to be Made "Variation-Aware"](chart.png)

9. Summary and Financial Impact

Variation-aware design was cited as the top segment of custom IC design where technology advancement is needed over the next 2 years. Designers named the top existing custom IC design tools they wanted to be made “variation-aware” to be layout editors, followed by true SPICE simulators, fast SPICE simulators, and then schematic capture.

The top two reasons respondents gave for deploying variation-aware design systems were to improve parametric yield - performance, power and area, and to avoid respins. A substantial number of designers saw variation becoming important starting at the 90 nanometer process node, with a majority citing design variation as necessary at 65 nanometers.

Deployment of variation-aware design tools can be expected to double in 2011 with custom design moving to lower process geometries. A majority of engineers and managers noted that design variation has caused design and tapeout delays or respins; these factors cause increased engineering costs and reduced product revenue.

The financial impact resulting from managing variation issues for a representative 50 person engineering team can reach $5 million per year. Several factors contribute to this amount:

- For a 50 person engineering team with a cost of $10M/year, 22% additional overhead on designer’s time associated with managing variation equates to $2.2M annually. Variation design software that can cut this overhead in half through automation would result in a $1.1M savings.

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For the average product delay of approximately 2 months, assuming half the 50 person engineering team is involved with identifying and repairing the variation issues, the engineering development cost for a would increase by about $800K. If a complete re-spin is involved, it could conservatively add another $500K in costs.

For a new product expected to generate $50M in revenue, depending on the length of the entire product lifecycle, a product delay of 2 months could easily reduce product revenue by $3M. Commercial variation design technologies can reduce and even eliminate this delay risk.

A variation-aware custom IC design system has the potential to allow organizations to implement design projects with fewer resources and to pull in delivery timetables.

**Variation-Aware Design Whitepapers**

- Variation-Aware Custom IC Design
- Cadence Virtuoso with Solido for Variation-Aware Design
- Synopsys HSPICE with Solido for Variation-Aware Design
- Variation-Aware Custom IC Design for High-Sigma

**About Solido Design Automation**

Solido Design Automation, Inc. is a leading provider of variation-aware custom integrated circuit design software. Solido Variation Designer and application packages are used by custom IC designers spanning analog/RF, I/O, memory and standard cell digital library design teams, to improve design performance, parametric yield, and designer productivity. The privately held company is venture capital funded and has offices in the U.S.A., Canada, Japan and Europe. For further information, visit www.solidodesign.com.

**Amit Gupta, President and CEO, Solido Design**

As co-founder, President and CEO of Solido, Amit has driven research, development, commercialization and sales growth of its variation-aware custom IC design software. Prior to founding Solido, in 1999 he co-founded Analog Design Automation Inc. (ADA), a startup for semiconductor design software. Over the next five years, as President and CEO and VP Marketing and Business Development, Amit managed the company’s development and launch its analog optimization products, revenue growth and acquisition by Synopsys Inc. Prior to becoming an entrepreneur, Amit was product manager for the wireless group at Nortel Networks and a hardware engineer for the RF Communications group at Harris Corporation. He graduated with degrees in both Electrical Engineering and Computer Science with great Distinction from the University of Saskatchewan. He was awarded the 2005 outstanding alumni award for significant accomplishments since graduation.

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