

Understanding MOSFET Mismatch for Analog Design

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Abstract

This paper addresses misconceptions about MOSFET mismatch for analog design. V_t mismatch does not follow a simplistic $1/(\sqrt{\text{area}})$ law, especially for wide/short and narrow/long devices, which are common geometries in analog circuits. Further, V_t and gain factor are not appropriate parameters for modeling mismatch. A physically based mismatch model can be used to obtain dramatic improvements in prediction of mismatch. This model is applied to MOSFET current mirrors to show some non-obvious effects over bias, geometry, and multiple unit devices.

I. Introduction

Mismatch is the time-independent differential performance of two or more devices. It is widely recognized that mismatch is key to precision analog IC design. Historically, mismatch has been treated as an "art" rather than a science, relying on past experience and unproven or uncharacterized effects. Exacerbating the situation is a fundamental lack of modeling and understanding of mismatch over bias and geometry. Without an accurate mismatch model, designers are forced to include substantial design margin or risk yield loss [1], both of which cost money and time. This paper highlights many of the perils of mismatch modeling and characterization based on experiences and discoveries at Motorola over the past eight years.

II. The Mismatch Model

The first reasonable mismatch model was proposed in [2], [3]. Here, the notion of global and local variations were introduced, as Fig. 1 shows. Global variation is independent of length L and width W . For local variation, the variation of L depends on the width of the device,

$$\sigma_L^2 \propto 1/W \text{ and likewise, } \sigma_W^2 \propto 1/L. \quad (1)$$

Parameters such as sheet resistance, channel dopant concentration, mobility and gate oxide thickness have

$$\sigma_p^2 \propto 1/(LW) \quad (2)$$

where the subscript p represents the parameter of interest. Physically, the edge variation in (1) and area dependent variation in (2) result from polysilicon/metal edge grains, photoresist edge roughness, dopant clustering, gate oxide thickness/permittivity variations, etc. Qualitatively, local variations decrease as the device size increases since the parameters "average" over a greater distance or area. As per [4], mismatch (i.e. intradie parameter variation) is dominated by local variation but traditional interdie

variation, used for best-case and worst-case models, contains both global and local components, although this is rarely accounted for.

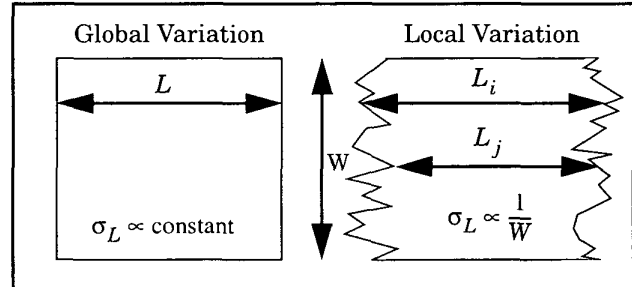


Fig. 1: Global variation and local variation. For local variation, the variance in length depends on the width.

The model in (1) was derived by evaluating the local length (e.g. L_i and L_j in Fig. 1) across the entire width and finding the second moment (i.e. the standard deviation) of the effective length.

An alternative derivation [5] has been used to describe mismatch behavior over geometry. This model assumes that the observed variation for a given parameter is the convolution of the small signal parameter spatial variation over the device area. Note that this model is identical to (2). Perimeter contributions to mismatch were not addressed in [5] but a similar derivation results in (1).

Although the model in [5] was derived correctly, it is incorrectly applied to threshold voltage V_t and gain factor β . These two parameters are combined to produce the I_d mismatch,

$$\sigma_{I_d}^2 = \sigma_\beta^2 + 4\sigma_{V_t}^2/(V_{gs} - V_t)^2. \quad (3)$$

One immediately apparent problem is the physical basis for these parameters. As pointed out in [6] and later in [7], if the underlying cause for mismatch variation is the gate oxide thickness t_{ox} , it will be accounted for in both V_t and β , thus σ_{I_d} will be overestimated by a factor as large as 2.

For mismatch modeling, one can consider two types of parameters: process and electrical (see Table 1). Process parameters are those physically independent parameters that control the electrical behavior of a device. Electrical parameters are those parameters that are of interest to the designer. V_t does not belong to either category.

V_t depends on t_{ox} , V_{fb} , N_{sub} , L and W . This means that relationship from [5],

$$\sigma_{V_t} = A_{V_t}/\sqrt{LW} \quad (4)$$

is physically incorrect, and measured data from many technologies confirm this. [10] tried to accommodate

Table 1: Relevant process and electrical parameters.

Process Parameters	Electrical Parameters
Flatband Voltage (V_{fb})	Drain current (I_d)
Mobility (μ)	Input voltage (V_{gs})
Substrate Dopant Conc. (N_{sub})	Trans-conductance (g_m)
Length Offset (ΔL)	Output Conductance (g_o)
Width Offset (ΔW)	
Short Channel Effect (V_{tl})	
Narrow Width Effect (V_{tw})	
Gate Oxide Thickness (t_{ox})	
Source/Drain Sheet Resistance (ρ_{sh})	

the otherwise anomalous scaling behavior by using the effective length and width (i.e. $L_{eff} = L - \Delta L$), but this is not appropriate for the same reason that short and narrow channel effects are not modeled with just with ΔL and ΔW .

Often V_t mismatch is assumed to be an electrical parameter, input offset voltage mismatch $\sigma_{V_{gs}}$. But

$$\sigma_{V_{gs}} = \sigma_{I_d} / g_m. \quad (5)$$

Even using the simplistic mismatch relationship in (3), it is apparent that $\sigma_{V_{gs}}$ is not the input offset voltage since neither σ_{I_d} nor g_m is constant over bias, yet $\sigma_{V_{gs}}$ is. The consequences of this distinction will be made apparent in section III.

Inadequate geometry selection hides the shortcomings of (4). Several different gate areas are used to extract the A_V coefficient in (4). Often, e.g. [5], these geometries are selected about $L = W$. This establishes a self-fulfilling situation in which an erroneous model appears to fit data well since no alternative models can be evaluated. Analog design uses wide/short and narrow/long devices, where there is no geometric sampling in [5] and the mismatch prediction error is large. A more complete geometric sampling should be used to test alternative mismatch models and detect unexpected mismatch behavior [9].

The most physically complete and accurate mismatch model is given in [7] for MOSFETs and [8] for BJTs. All mismatch models are based on the Propagation of Variance (POV) relationship,

$$\sigma_e^2 = \sum_i \left(\frac{\partial e}{\partial p_i} \right)^2 \sigma_{p_i}^2 \quad (6)$$

where e is any electrical parameter and p is the list of process parameters, see Table 1. For MOS mismatch models other than [7] the partial derivatives in (6) are based on the simplistic I_d model

$$I_d = 0.5\beta(V_{gs} - V_t)^2, \quad (7)$$

or extensions of (7), with V_t and β as process parameters, and I_d as the electrical parameter.

The mismatch model in [7] is more complete since it uses BSIM3 (or any other SPICE MOSFET model) to evaluate the partial derivative in (6), which is substantially more accurate than using a simple analytic model like (7). Unlike the mismatch model in (3), [7] is valid in the linear and saturation regions, for sub-threshold, weak inversion and strong inversion condi-

tions, and for all geometries. A partial comparison of the modeling approaches is given across bias in Fig. 2 and across geometry in Fig. 3, for a nMOS device in a 0.25 μ m CMOS technology. Clearly there is a significant improvement of the model [7] over the standard approach (3) and (4). A detailed discussion of the characteristics of these plots is given in [7].

Applying (6) to MOSFETs produces (8) on the next page. The tilde (\sim) above a variable indicates a normalized parameter. For characterization, the vector on the left side of (8) is a set of I_d mismatch standard deviations collected across many die for many biases and geometries, typically hundreds of combinations. The combinations are chosen so that the process parameter mismatch variances are observable in the I_d mismatch data, with a unique and unconfounded solution. For instance, ρ_{sh} only significantly affects I_d for short devices in the linear region for high V_{gs} , so we measure mismatch under these conditions.

The large matrix in (8) contains the squares of the sensitivities of I_d with respect to each of the process parameters. Each row of sensitivities is numerically evaluated using SPICE at the bias and geometry conditions at which the corresponding σ_{I_d} is measured.

Given the first two matrices in (8), the right-most vector of process parameters can be calculated using analytic, simple linear regression. This method is called Back Propagation of Variance (BPV). Note that the process parameters in the right-side vector of (8) contain the local variation geometric scaling as prescribed by (1) and (2). This means that geometric scaling is applied to both the variance and the sensitivity components on the right side of (6). The geometric scaling affects the sensitivities through the underlying SPICE MOSFET model.

III. Mismatch application

An accurate mismatch model is not practical unless it can be used for design. We use MOSFET current mirrors to illustrate some non-obvious mismatch phenomena. Similar analysis can be used for other applications such as differential pairs.

A. Geometry and bias inter-relationship

What is the best way to size devices in a current mirror to meet matching requirements? A MOSFET current mirror is biased with a current, so the gate voltage depends on geometry. Intuitively, as the gate overdrive voltage $V_{od} = V_{gs} - V_t$ increases, those parameters that effect V_t have less impact on the I_d mismatch. This is even apparent in (3).

As L increases, the intrinsic mismatch decreases as per (1) and (2), but at the same time V_{pd} increases to supply the same reference current. Therefore the sensitivity component in (6) also decreases, constructively combining to further decrease σ_{I_d} .

As W increases, the intrinsic mismatch decreases, but V_{od} decreases. These two effects offset each other, and as Fig. 4 shows can give rise to little or no improvement in mismatch with increasing W . Depending on the underlying dominant mismatch process parameters, better matching can be obtained,

without consuming additional area, just by changing the W/L aspect ratio. This improvement comes at the expense of reduced dynamic range since V_{od} increases and hence the linear/saturation transition point for V_{ds} (V_{dsat}) increases.

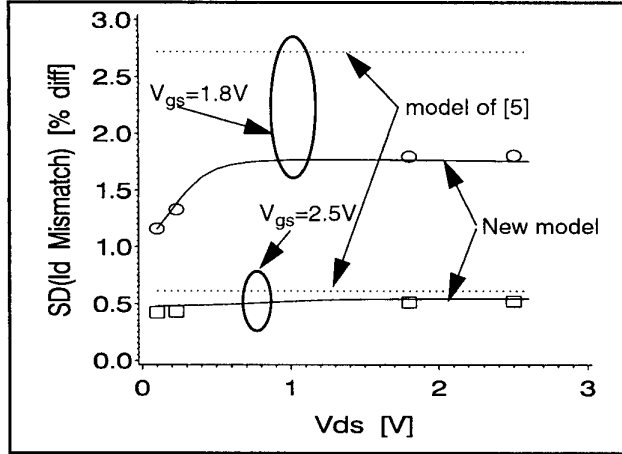


Fig. 2: nMOS I_d mismatch over bias, $0.25\mu\text{m}$ CMOS technology, $W/L=7/0.56\mu\text{m}$ $V_{bs}=-2.5\text{V}$. Symbols are data.

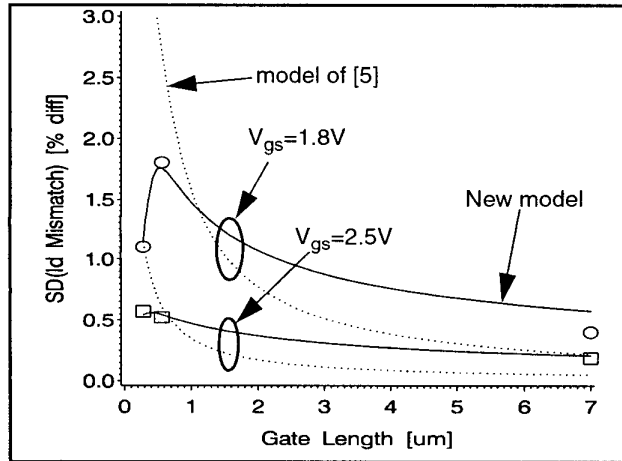


Fig. 3: nMOS I_d mismatch vs. L , $0.25\mu\text{m}$ CMOS technology, $W=7\mu\text{m}$, $V_{ds}=2.5\text{V}$ $V_{bs}=-2.5\text{V}$. Symbols are data.

For graded channel MOSFETs [11], the geometry and bias trade-off can have a much more profound impact, as Fig. 5 shows. A cut along $L=25\mu\text{m}$ in Fig. 5 shows that the underlying dominant cause for mismatch changes as W changes, see Fig. 6.

The impact of V_{od} on mismatch also means that mismatch is not constant if the reference current is not constant, such as in an active load, see Fig. 7.

So current mirror mismatch depends strongly on L and not W . Proper sizing of MOSFETs in current mirrors requires a mismatch model that is accurate over both bias and geometry.

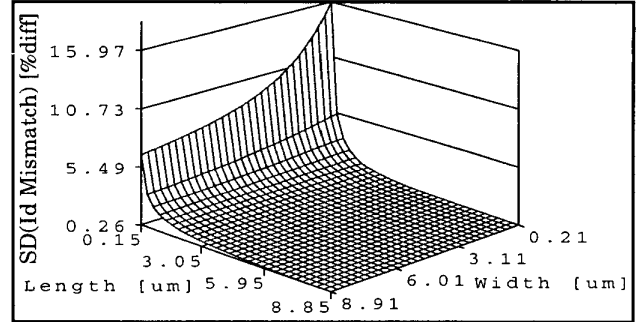


Fig. 4: 3-D plot of I_d mismatch vs. L and W for an nMOS current mirror, $I_{ref}=10\mu\text{A}$, $0.13\mu\text{m}$ CMOS technology.

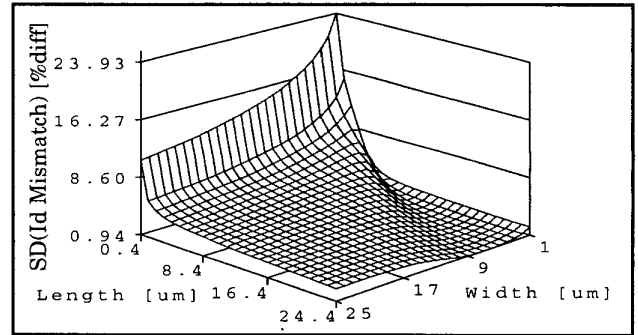


Fig. 5: 3-D plot of I_d mismatch vs. geometry, graded channel nMOS, at $I_{ref}=10\mu\text{A}$, $0.25\mu\text{m}$ BiCMOS technology.

$$\begin{bmatrix} \sigma_{I_{d1}}^2 \\ \sigma_{I_{d2}}^2 \\ \sigma_{I_{d3}}^2 \\ \dots \\ \sigma_{I_{dn}}^2 \end{bmatrix} = \begin{bmatrix} \left(\frac{d\tilde{I}_{d1}}{d\Delta W} \right)^2 & \left(\frac{d\tilde{I}_{d1}}{dt_{ox}} \right)^2 & \left(\frac{d\tilde{I}_{d1}}{dV_{fb}} \right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{\mu}_o} \right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\Delta L} \right)^2 & \left(\frac{d\tilde{I}_{d1}}{dV_{tl}} \right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{\rho}_{sh}} \right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{N}_{sub}} \right)^2 \\ \left(\frac{d\tilde{I}_{d2}}{d\Delta W} \right)^2 & \left(\frac{d\tilde{I}_{d2}}{dt_{ox}} \right)^2 & \left(\frac{d\tilde{I}_{d2}}{dV_{fb}} \right)^2 & \left(\frac{d\tilde{I}_{d2}}{d\tilde{\mu}_o} \right)^2 & \left(\frac{d\tilde{I}_{d2}}{d\Delta L} \right)^2 & \left(\frac{d\tilde{I}_{d2}}{dV_{tl}} \right)^2 & \left(\frac{d\tilde{I}_{d2}}{d\tilde{\rho}_{sh}} \right)^2 & \left(\frac{d\tilde{I}_{d2}}{d\tilde{N}_{sub}} \right)^2 \\ \left(\frac{d\tilde{I}_{d3}}{d\Delta W} \right)^2 & \left(\frac{d\tilde{I}_{d3}}{dt_{ox}} \right)^2 & \left(\frac{d\tilde{I}_{d3}}{dV_{fb}} \right)^2 & \left(\frac{d\tilde{I}_{d3}}{d\tilde{\mu}_o} \right)^2 & \left(\frac{d\tilde{I}_{d3}}{d\Delta L} \right)^2 & \left(\frac{d\tilde{I}_{d3}}{dV_{tl}} \right)^2 & \left(\frac{d\tilde{I}_{d3}}{d\tilde{\rho}_{sh}} \right)^2 & \left(\frac{d\tilde{I}_{d3}}{d\tilde{N}_{sub}} \right)^2 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ \left(\frac{d\tilde{I}_{dn}}{d\Delta W} \right)^2 & \left(\frac{d\tilde{I}_{dn}}{dt_{ox}} \right)^2 & \left(\frac{d\tilde{I}_{dn}}{dV_{fb}} \right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\tilde{\mu}_o} \right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\Delta L} \right)^2 & \left(\frac{d\tilde{I}_{dn}}{dV_{tl}} \right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\tilde{\rho}_{sh}} \right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\tilde{N}_{sub}} \right)^2 \end{bmatrix} \begin{bmatrix} \sigma_{\Delta W}^2 / L \\ \sigma_{t_{ox}}^2 / (LW) \\ \sigma_{V_{fb}}^2 / (LW) \\ \sigma_{\tilde{\mu}_o}^2 / (LW) \\ \sigma_{\Delta L}^2 / W \\ \sigma_{V_{tl}}^2 / W \\ \sigma_{\tilde{\rho}_{sh}}^2 / (LW) \\ \sigma_{\tilde{N}_{sub}}^2 / (LW) \end{bmatrix} \quad (8)$$

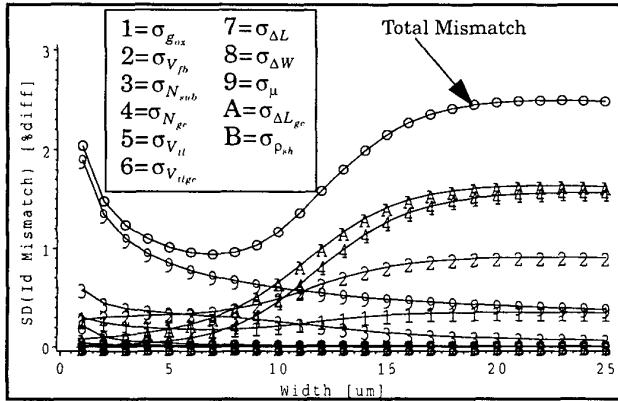


Fig. 6: I_d mismatch and the underlying process parameter contributions for $L=25\mu\text{m}$ in Fig. 5. "gc" subscript indicates parameters specific to the graded channel.

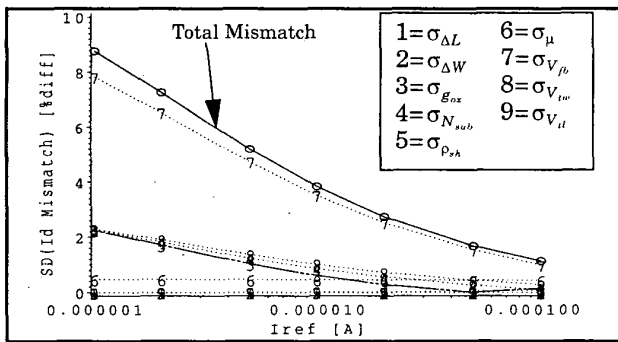


Fig. 7: Current mirror I_d mismatch vs. I_{ref} , $W/L=2/2\mu\text{m}$, $0.13\mu\text{m}$ CMOS technology.

B. nMOS or pMOS?

A common question is, "Which matches better, nMOS or pMOS?" The answer depends on how a device is biased. With voltage bias there is no consistent trend across technologies.

With current bias, the lower mobility for pMOS means that a larger V_{od} is required to supply the same reference or tail current. Table 2 shows this for standard logic nMOS and pMOS devices in a $0.4\mu\text{m}$ power BiCMOS process. So for a fixed current pMOS gives better matching because of higher V_{od} .

Table 2: Mismatch for $2\times 2\mu\text{m}^2$ nMOS and pMOS devices on a $0.4\mu\text{m}$ power BiCMOS process.

Bias Condition	Device	V_{gs} [V]	SD(Id Mismatch) [%diff]
Current Mirror $I_{ref}=10\mu\text{A}$	nMOS	1.09	1.22%
	pMOS	1.70	1.09%
Voltage Driven $V_{gs}=1.70\text{V}$	nMOS		0.589%
	pMOS		1.09%

C. Ratio up or ratio down?

Where integer current scaling is desired, the matching of a 1:n ratio differs from a n:1 ratio. If n devices are placed in parallel, each device contributes additional mismatch variance. The process parameter variances in (6) increases by n, but the squared sensitivities decrease by a factor of n^2 , so σ_{I_d} decreases by

a factor of \sqrt{n} . The situation for current mirrors is slightly different since multiple unit devices in the reference transistor are mapped through the gate voltage. As Table 3 shows, the majority of the improvement from multiple parallel device is gained by using them for the output, not the reference, MOS.

Table 3: Impact of multiple unit devices on current mirror mismatch for an $2\times 2\mu\text{m}^2$ nMOS device on a $0.13\mu\text{m}$ CMOS process. I_{ref} is scaled for the reference device to maintain constant voltage bias.

# in parallel reference device	# in parallel output device	SD(Id Mismatch) [%diff]
1	1	3.86
1	4	1.52%
4	1	3.05%
4	4	1.41%

D. Linear versus saturation region

It is desirable to keep the output device of a current mirror in saturation to maintain high g_o . But as supply voltages decrease, mirrors can enter the linear region. For a voltage driven MOSFET, as Fig. 2 shows, the I_d mismatch decreases in the linear region. When placed in a mirror, this improvement is offset by contributions to the mismatch from the output conductance of the output device in the linear region. So, for a current mirror, I_d mismatch remains virtually unchanged over the entire V_{ds} bias range.

IV. Conclusions

Mismatch is important for analog IC design, and accurate mismatch modeling is necessary to avoid parametric yield loss and over-design. The common approach to mismatch modeling, based on V_t and β , leads to inaccurate predictions over geometry and bias. Mismatch modeling based on physical process parameters is significantly more accurate.

V. References

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