

A Comprehensive MOSFET Mismatch Model

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Abstract

This paper presents a new model for MOSFET mismatch, based on physical process parameters and characterization by backward propagation of variance. Experimental data show significantly more accurate modeling of MOSFET mismatch over geometry and bias than previously reported models. The new approach allows identification of the fundamental cause of mismatch, for process diagnosis.

Introduction

Mismatch is a leading cause of parametric yield loss and a determining factor of circuit performance, such as bit resolution, in analog-mixed signal (AMS) ICs. Low risk design thus requires accurate modeling and characterization of mismatch. Most MOSFET mismatch models are based on the work of Pelgrom et al. [1]. However, this approach does not have a proper physical foundation, is inaccurate over geometry and bias, and does not account for important root causes of mismatch in modern sub-micron CMOS technologies. In at least one instance, [4], a 2-X error in mismatch prediction from the Pelgrom model has been cited as the reason for bit resolution loss in a data converter design.

Primarily, [1] and similar models are based on SPICE model parameters, V_{th} and $\beta = \mu_0 C_{ox} W/L$ (or $k_p = \mu_0 C_{ox}$), with a $1/WL$ geometry dependence. Yet it is variations in physical process parameters, p_j , such as V_{fb} , T_{ox} , Δ_L , Δ_W , μ_0 , and N_{sub} that cause mismatch. Correlations, e.g. of V_{th} and β through T_{ox} , are ignored in previous models, leading to inaccurate modeling of mismatch for some technologies. Other problems are that V_{th} and β are characterized in the linear region, yet most analog CMOS circuits operate in saturation, and MOSFET mismatch is observed to be inadequately modeled as varying with geometry as $1/WL$. Finally, the common assumption that input offset voltage of differential pairs is equivalent to V_{th} mismatch is incorrect. V_{gs} mismatch, which is the input offset voltage, at a fixed I_d is also affected by other process parameters, such as those listed previously. In some cases, process parameters that determine the V_{th} mismatch may have only a small contribution to the input offset voltage mismatch.

The purpose of this work is to present a new and improved approach to modeling MOSFET mismatch. The new model advances the state of the art because it is based on physical process parameters, rather than SPICE model parameters, and it is characterized from measurements of drain current mismatch, rather than from direct measurement of the mismatch parameters.

This gives accurate modeling of mismatch in a manner most relevant to circuit design. The new model is verified with extensive measurements, and demonstrated to be more accurate than previous models.

Method

Besides the process parameters listed above, the source and drain region sheet resistance ρ_{sh} and the length variation of threshold V_{tl} are included in our model. The process parameters are mapped into SPICE model parameters, e.g. by defining V_{th} as a function of V_{fb} , T_{ox} , and N_{sub} ,

$$\Delta_a V_{th} = \Delta_a V_{fb} + 2 \frac{kT}{q} \ln(\Delta_r N_{sub}) + \frac{2T_{ox} \sqrt{N_{sub} \epsilon_{Si} \epsilon_0 kT \ln\left(\frac{N_{sub}}{n_i}\right)}}{\epsilon_{ox} \epsilon_0} \left[(\Delta_r t_{ox}) \sqrt{(\Delta_r N_{sub}) \left(\frac{\Delta_r N_{sub} - 1}{\ln\left(\frac{N_{sub}}{n_i}\right)} + 1 \right)} - 1 \right] \quad \text{Eq. (1)}$$

where the operators, Δ_a and Δ_r denote the difference and relative difference of a given parameter. The mismatch variances σ^2 of the p_j are mostly modeled as having $1/WL$ and s^2 components, where s is the spacing between device centroids. Δ_L and Δ_W do not vary as inverse area, but have constant and $1/W$ and $1/L$ terms, respectively. Via the sensitivities of electrical performances to process parameters this implicitly introduces $1/L^2$, $1/WL^2$, $1/W^2$, and $1/LW^2$ geometry variations in simulated mismatch. ρ_{sh} and V_{tl} do not vary with length so their mismatch variances have $1/W$ scaling rather than inverse area scaling.

The mismatch variances of p_j are not characterized directly. Rather, mismatch in I_d is measured over geometry and bias (linear and saturation regions), and the σ^2 in the p_j are calculated from backward propagation of variance (BPV, [2,3]),

$$\sigma_{I_d}^2 = \sum_j (\partial I_d / \partial p_j)^2 \sigma_{p_j}^2, \quad \text{Eq. (2)}$$

measure $\sigma_{I_d}^2$, simulate $\partial I_d / \partial p_j$, calculate $\sigma_{p_j}^2$

where the sensitivities $\partial I_d / \partial p_j$ are computed from the SPICE models for each bias and geometry. Note that in this approach the variation in Δ_L has a larger effect for

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short channel devices, as is physically expected and observed in data.

Results

Conventional analysis based on the Pelgrom model [1] gives

$$\sigma_{I_d}^2/I_d^2 = \sigma_{\beta}^2/\beta^2 + 4\sigma_{V_{th}}^2/(V_{gs} - V_{th})^2. \quad \text{Eq. (3)}$$

Figs. 1, 2, and 3 compare results of the Pelgrom model and Eq. (3), results from the new model, and measured data from a 0.28 μm CMOS technology. Qualitatively, the Pelgrom model shows the correct trend over V_{gs} , given by the second term in Eq. (3), but quantitatively the new model is much more accurate. The Pelgrom approach does not model the transition to the linear region in Fig. 1. The new model correctly predicts the reduction in mismatch in the linear region, including its V_{gs} and V_{bs} dependence. "Anomalous" behavior over length and width that is not even qualitatively accounted for by the Pelgrom model is well modeled by the new approach, see Figs. 2 and 3. In Fig. 2, as the channel length shrinks the body effect shrinks, the mismatch becomes less sensitive to variations in N_{sub} , so this component should reduce and the mismatch should decrease, especially at high V_{bs} . This is seen in the data, and can be modeled only by our new approach. The "crossover" in Fig. 3 is caused by mismatch in ρ_{sh} , which has the greatest effect at low V_{ds} and high V_{gs} , where the channel resistance is least relative to the parasitic series resistance. Our approach models this, previous approaches do not.

Table 1 shows the extracted mismatch model coefficients for the nMOS and the complementary pMOS devices. Comparisons to evaluate the relative contributions to the mismatch from each of the process parameters should not be made in terms of these extracted coefficients. As shown in Eq. (2), the mismatch contribution is the product of the model coefficient and the squared sensitivity. The former has a geometry dependency, and the latter has a geometry and bias dependency, which implies that the process parameter mismatch contributions need to be evaluated per bias and geometry combination. Fig. 4 shows an example of this, where the contributions of each of the process parameters and the overall device mismatch are plotted against device width. These plots allow, for the first time, identification of the dominant root causes of mismatch for specific technologies. ρ_{sh} mismatch dominates for low V_{ds} and high V_{gs} , and V_{fb} is important elsewhere. In saturation V_{th} and Δ_L are significant for wide devices.

The predicted I_d mismatch for the complementary pMOS device, using the Pelgrom model, significantly overpredicts the measured mismatch values as shown in Fig. 5. This situation is created by a T_{ox} mismatch source. Since both the V_{th} and β mismatch terms in the Pelgrom model include T_{ox} independently, measured and extracted distributions of V_{th} and β produce a

"double measure" of the T_{ox} mismatch. This is consistent with the extracted T_{ox} mismatch coefficients in Table 1, assuming similar sensitivities for the nMOS and pMOS device. An independent correlation plot of V_{th} versus β for both the nMOS and pMOS devices confirmed the relationship. But, if these two device are complementary (implying that the gate oxides are grown simultaneously), why is the T_{ox} mismatch so different for the n and p devices? For the nMOS device, a slightly thicker gate oxide will leach more B dopant from the channel region. The increase in V_{th} created by the increase in T_{ox} is offset by the decrease in V_{th} due to the slightly lower channel dopant concentration. For the pMOS device, more P tends build up at the interface for a thicker T_{ox} , which are complementary in affecting V_{th} . Using this argument, nMOS devices will exhibit better mismatch than pMOS devices if the underlying cause for the mismatch is T_{ox} .

TABLE 1. Extracted mismatch model coefficients.

Parameter	nMOS	pMOS
σ_{Δ_w} [$\mu\text{m}^{3/2}$]	1.261	1.083
$\sigma_{t_{ox}}$ [μm]	0.344	3.216
$\sigma_{V_{fb}}$ [$\text{V} \cdot \mu\text{m}$]	0.932	1.853
σ_{μ_o} [μm]	0.584	2.032
σ_{Δ_L} [$\mu\text{m}^{3/2}$]	0.0	0.0
$\sigma_{V_{th}}$ [$\text{V} \cdot \mu\text{m}$]	0.0	0.324
$\sigma_{\rho_{sh}}$ [μm]	5.790	0.0
$\sigma_{N_{sub}}$ [μm]	2.017	4.675

Conclusion

In summary, we present a new, physically based, accurate model for MOSFET mismatch. The model is able to both qualitatively and quantitatively represent measured mismatch behavior over bias and geometry that was not possible with previous models. This is verified over a significantly more comprehensive set of data than has been presented previously. A unique and powerful advantage of the new approach is that analysis of the contributions of the process parameters to the overall mismatch allows identification of the most important physical root causes of mismatch, which can be used to guide process diagnosis and improvement.

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- [2] P. Drennan, C. McAndrew, J. Bates, "A comprehensive vertical BJT mismatch model," *IEEE BCTM98*.
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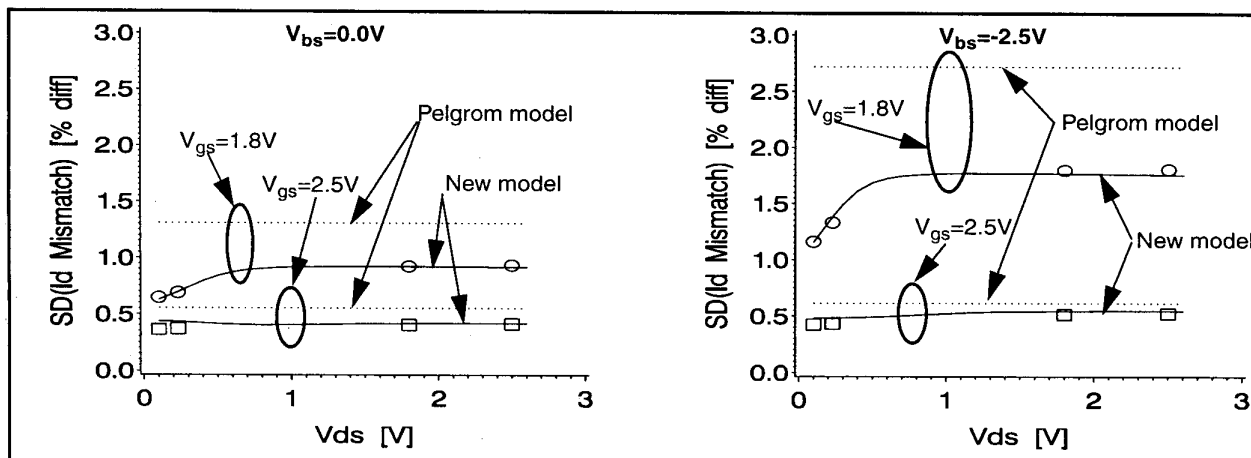


Fig. 1 nMOS I_d mismatch over bias, $W/L=7/0.56\mu m$. Circles are data for $V_{gs}=1.8V$ and squares are for $V_{gs}=2.5V$.

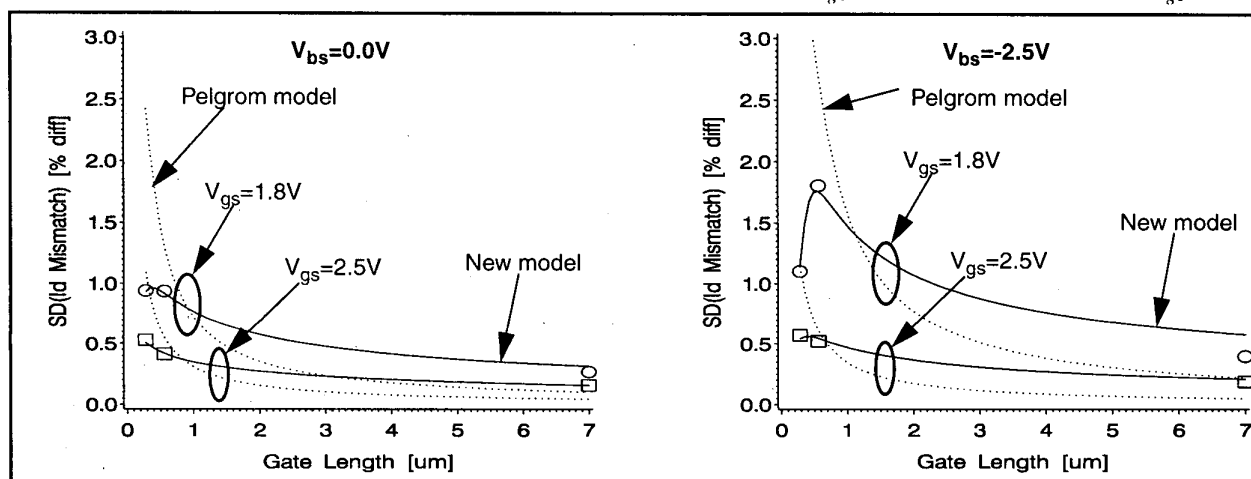


Fig. 2 nMOS I_d mismatch vs. L , $W=7\mu m$, $V_{ds}=2.5V$. Circles are data for $V_{gs}=1.8V$ and squares are for $V_{gs}=2.5V$.

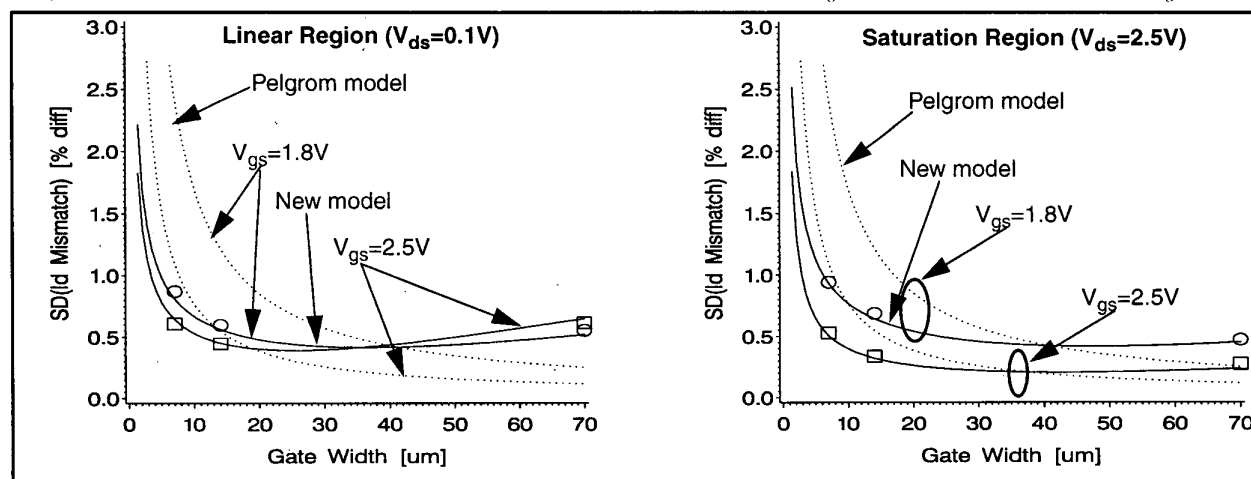


Fig. 3 nMOS I_d mismatch over W , $L=0.56\mu m$, $V_{bs}=0.0V$. Circles are data for $V_{gs}=1.8V$ and squares are for $V_{gs}=2.5V$.

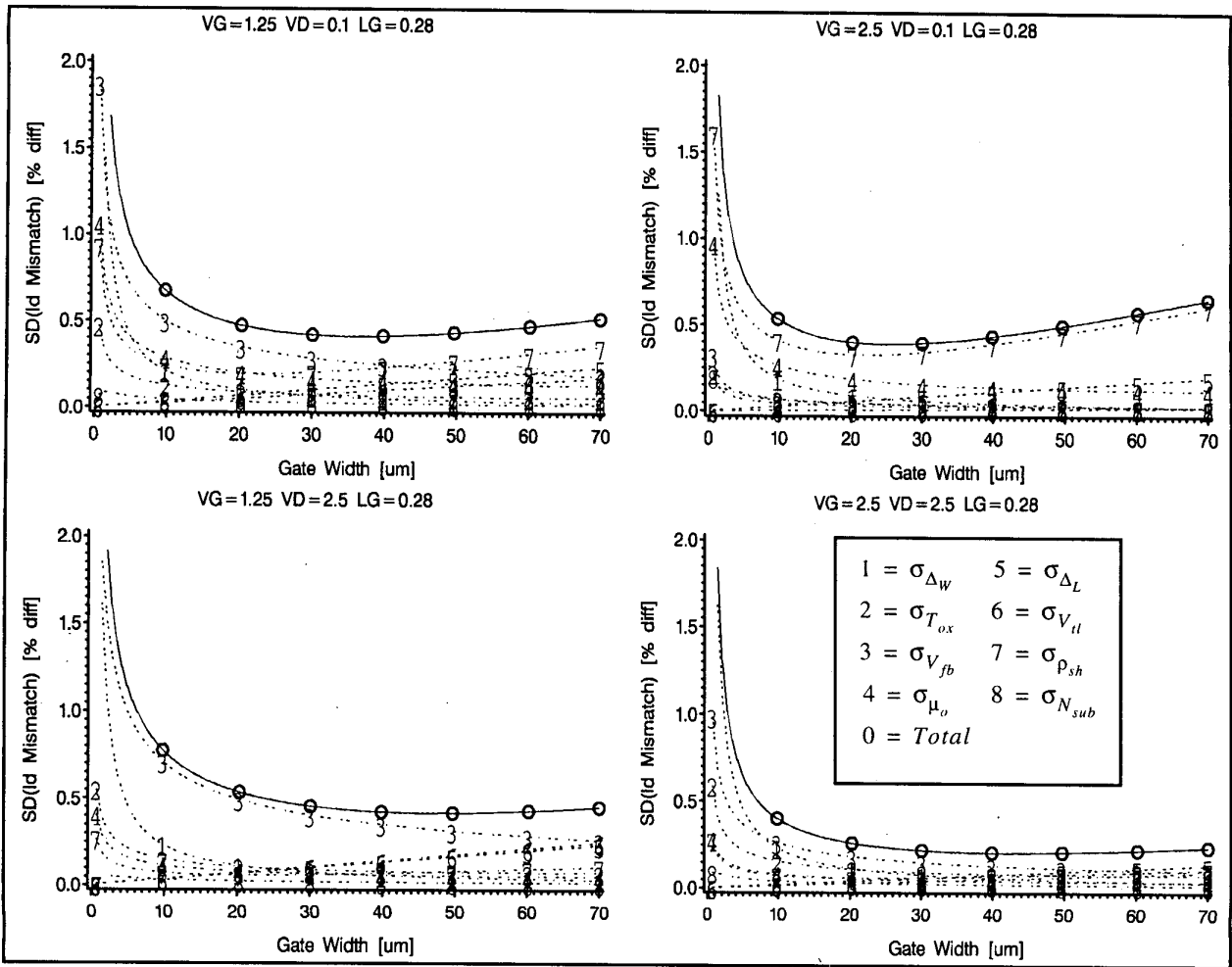


Fig. 4 Plots of the process and geometry components of I_d mismatch versus W for the plots in Fig. 3. Note that standard deviation (SD) is plotted, but the variances add so the solid total mismatch SD is the root sum of squares of the components.

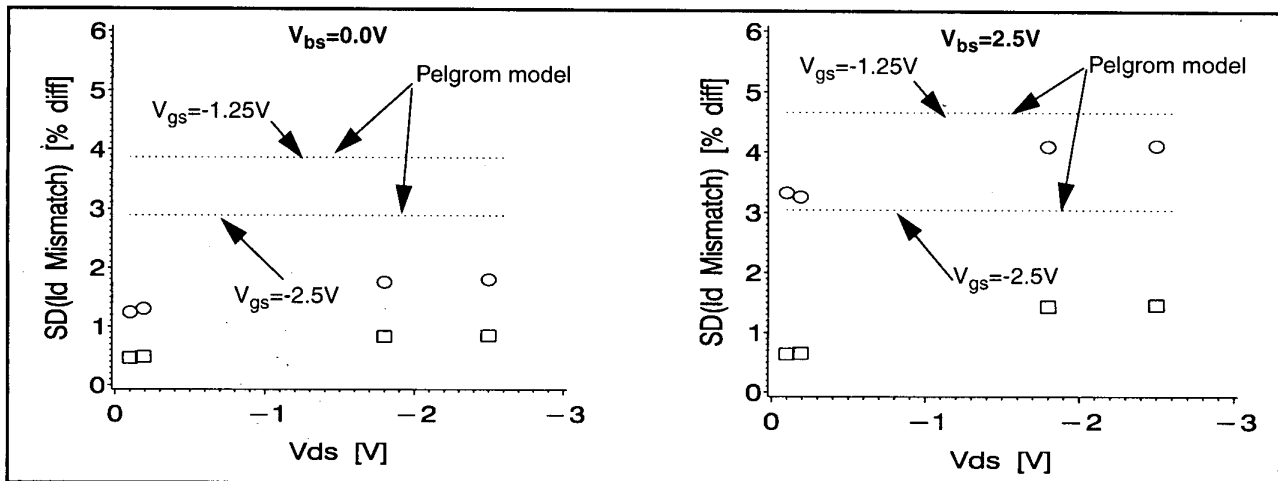


Fig. 5 pMOS I_d mismatch vs. bias, $W/L=7/0.56\mu\text{m}$. Circles are data for $V_{gs}=-1.25\text{V}$ and squares are for $V_{gs}=-2.5\text{V}$.

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