

SolidoSTAT:

Transistor-Level Statistical Design and Verification Tool Suite

Overview:

Process variation costs money. At today's geometries, statistical effects are difficult to design around and cause more and more semiconductor designs to yield badly.

For analog/mixed-signal, custom digital, and memory designs, it has become an industry standard to use Monte Carlo analysis to predict design yield in the presence of statistical process variation. When specifications are not met, however, it can be difficult for designers to efficiently improve the design. Under project time pressure, designers are often forced to build in large margins, sacrificing area, power, and performance for robustness where possible.

Instead, transistor-level designers need an efficient way to gain insight into the effects of process variation on their design and make the design robust to these effects. The SolidoSTAT tool suite from Solido Design Automation puts these capabilities in the transistor-level designer's hands.

SolidoSTAT Sampler:

The SolidoSTAT Sampler is an essential productivity tool for statistical design and verification. It increases Monte Carlo analysis productivity by employing superior sampling algorithms, automating parallel sampling, providing instant run-time feedback, and displaying results using targeted visualizations that answer key design questions.

SolidoSTAT Tradeoff Analyzer:

The SolidoSTAT Tradeoff Analyzer mines Sampler results to automatically identify tradeoffs between specifications and yield. This tool makes the designer aware of options for altering specifications in minutes without performing any additional simulations.

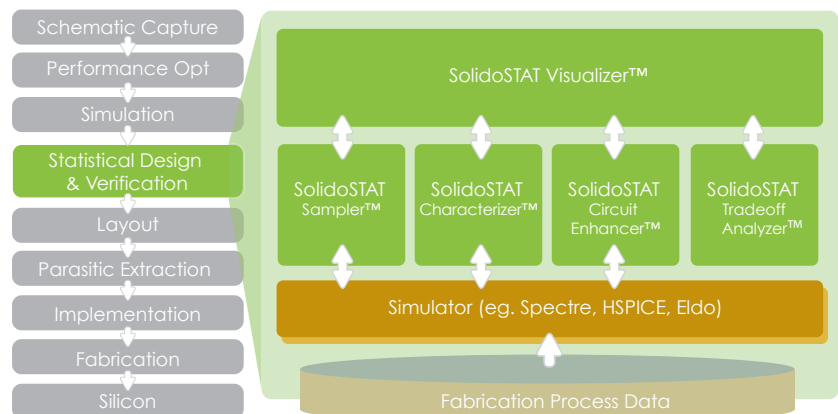
SolidoSTAT Characterizer:

The SolidoSTAT Characterizer pinpoints the effects that impact yield and performance in the design using advanced, efficient algorithms. It identifies causes of problematic

Figure 1:

The SolidoSTAT tool suite.

The Sampler, Characterizer, and Circuit Enhancer iterate with a SPICE simulator to explore the effects of process variation, while the Tradeoff Analyzer and Visualizer mine the data, providing the designer with additional insight.



variations, including devices, design variables, process variables, and environmental variables. Results are post-processed automatically and presented using intuitive visualizations.

SolidoSTAT Circuit Enhancer:

The SolidoSTAT Circuit Enhancer automatically improves the design to make it robust to statistical process variation. It presents multiple solutions, allowing the designer to explore many candidate solutions and choose the design most suitable for the application.

SolidoSTAT Visualizer:

The SolidoSTAT Visualizer is an information visualization package that is customized for the purposes of statistical design and verification. The Visualizer integrates seamlessly with the rest of the SolidoSTAT toolset, converting raw data from the various analyses into concise and meaningful representations that contribute to designer insight.

Features:

- Comprehensive statistical design and verification solution
- Powerful algorithms that combine speed and accuracy

- Rich visualizations designed specifically to answer transistor-level designer questions
- Simulator independent (support for Spectre, HSPICE, Eldo, and proprietary simulators)
- Seamless integration into Cadence Virtuoso/ Analog Design Environment
- Built-in parallel simulation environment
- Efficient and easy to use

Benefits:

- Improve robustness to process variation (i.e. higher yields)
- Accelerate Monte Carlo analysis
- Reduce circuit over-design
- Gain insight into the effects of process variation
- Increase designer productivity
- Make more effective use of circuit simulators
- Decrease time-to-market
- Apply a comprehensive methodology for addressing statistical process variation
- Perform statistical verification and signoff

Platforms Supported:

- Red Hat Enterprise 3 & 4 (Intel & AMD, 32 and 64 bit)
- Sun Solaris 8 & 10 (SPARC)

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